Timing System Operator Training

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Disclaimer

"This is a true story, although it may not have happened…"

— Preface to a Native American Creation Story

Basic Definitions

- Machine Cycle
  - A roughly 5 millisecond period of time occurring 60 times per second, during which a sequence of events may occur that culminate in the production, acceleration, and delivery of one pulse of beam. The start of a machine cycle has its origins in the positive zero-crossing of the 60 Hz line AC.
- Event Link
  - A serial line delivered to all front-end computers, on which the events that govern the timing of a machine cycle are transmitted.
- Event
  - An eight bit number transmitted on the event link that determines the timing of a particular step in the machine cycle.
- Timing Gate
  - A TTL signal, generated by the timing system, that actually controls some piece of equipment. A timing gate is typically generated at the front-end. It is triggered by an event from the event link. Local delays and widths are applied so that the gate will fire at the correct time relative to when the event is received.

Basic Definitions

- Real Time Data Link
  - A serial line delivered to all front-end computers, on which data relevant to the next machine cycle is transmitted. Data on the real time data link is transmitted 60 times per second, just prior to the start of a machine cycle.
- RTDL Frame
  - The basic unit of information transmitted on the Real Time Data Link. One RTDL frame consists of a 24-bit data word, and an 8-bit frame number that describes what the data represents.
- Turn
  - The fundamental unit of measurement of the timing system.
  - 1 turn = 1 ring revolution = 945 nSec (at 1 GeV).
  - Granularity of timing system is 1/32nd turn (about 30 nSec)

Two Goals

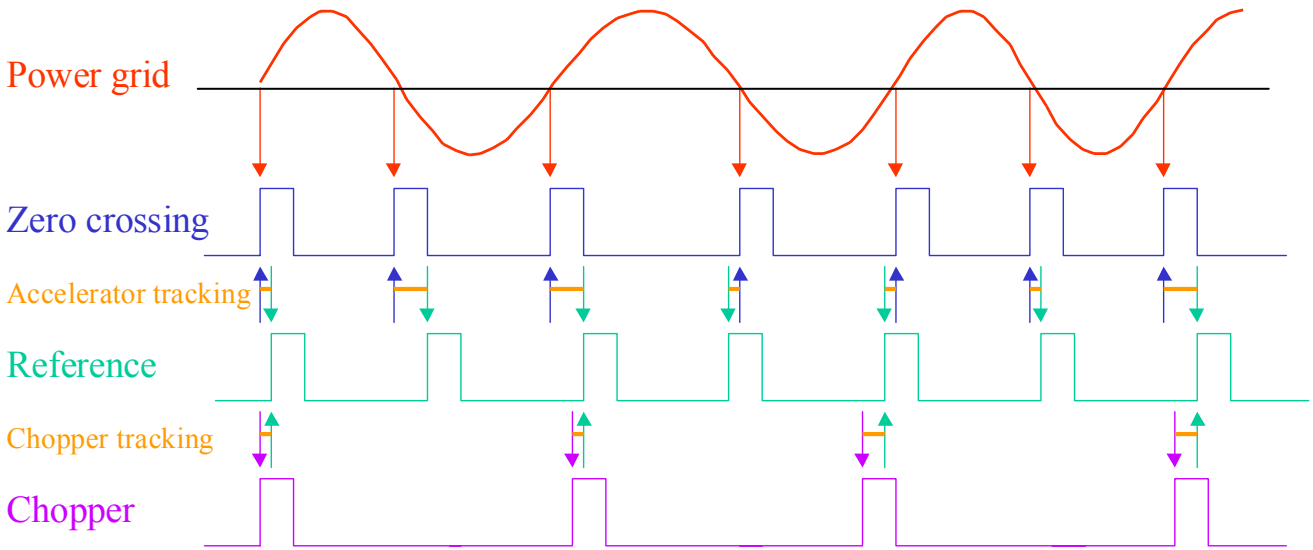
- Produce a very stable 60 Hz signal
  - Synchronize multiple neutron choppers (high inertia, slow response to change)
- Produce a 60 Hz signal synchronized with the AC line current.
  - Power supplies require phase lock

Compromise

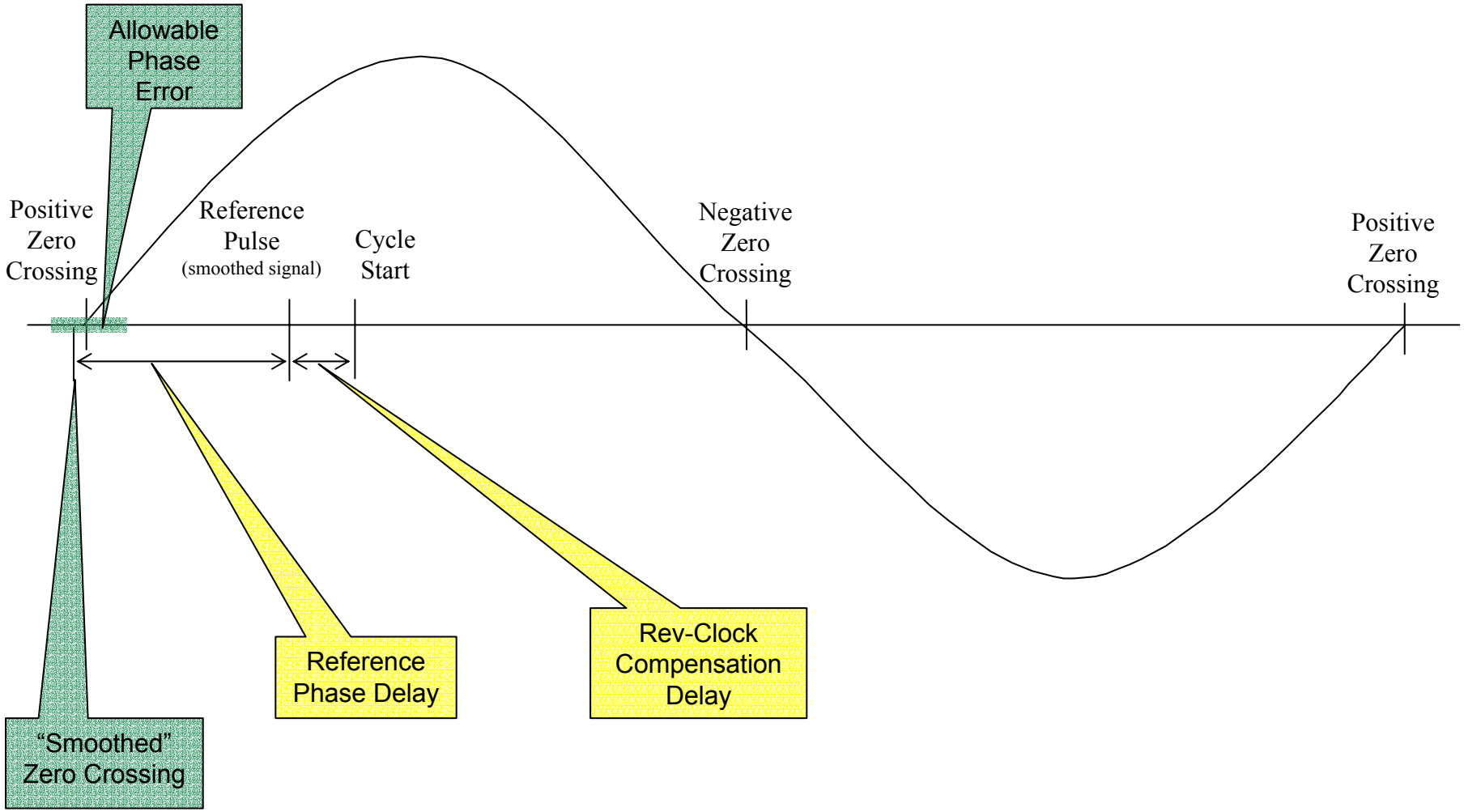
- Produce a relatively stable 60 Hz signal that does not change faster than the choppers can keep up with and that is phase-lock to the AC line within 500 μSec.

Timing Reference Generator

- Provides 60 / 120 Hz system pulses
- Follows line to within +/- 500 usec
- Neutron Choppers follow Timing Master (60 Hz system pulses)
- Accelerator timing follows Timing Master



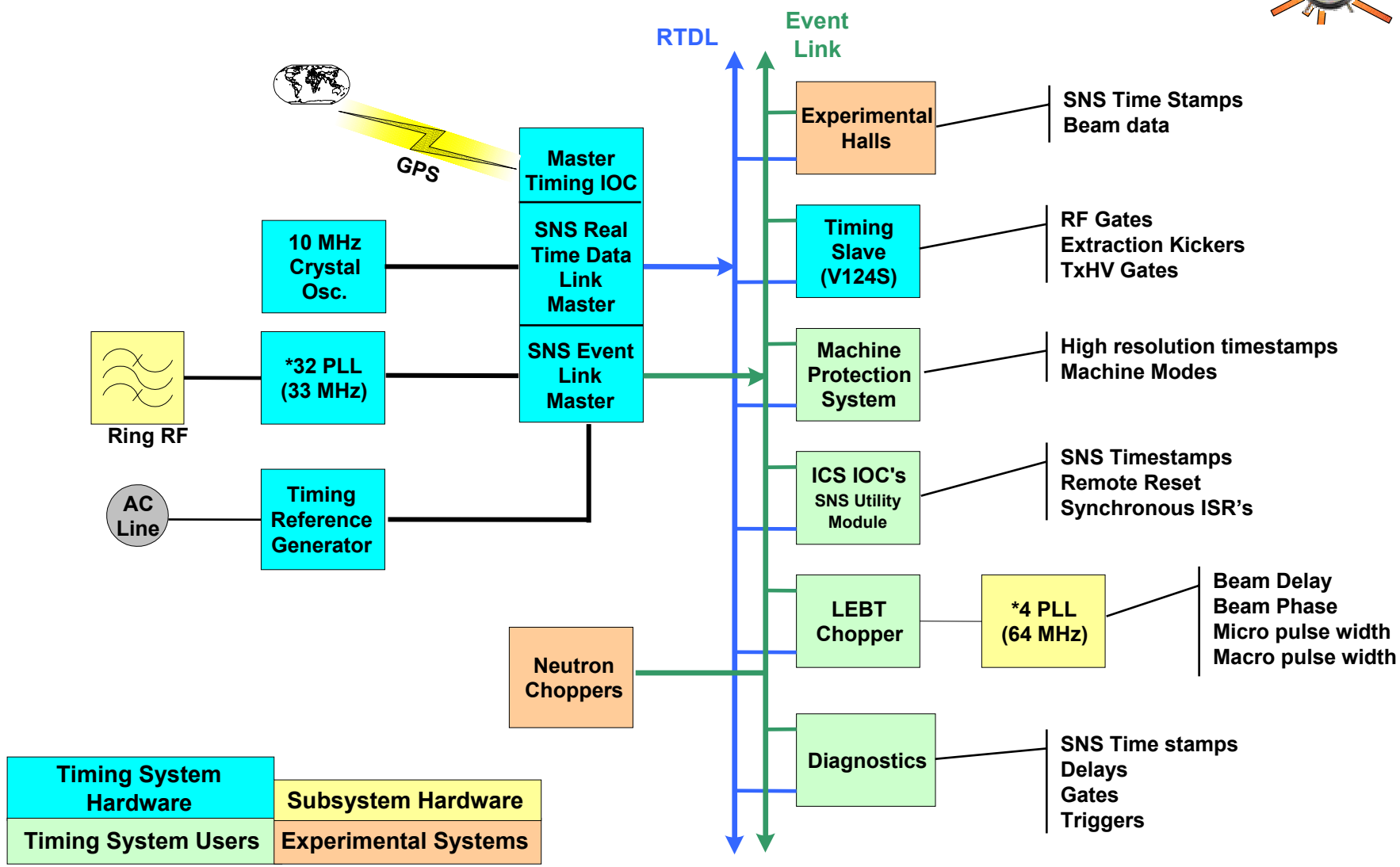
Timing Reference Generator — Timeline



Important Implication

- The beam injection, and all timing gates associated with it (source, RF, etc.) must always end at the same place in the machine cycle.
- This place is signaled by an event called “End Injection”
  - End Injection comes slightly before the extraction kickers fire
  - Guarantees that beam won’t “languish” in the ring waiting for extraction.
- If you want more beam, you must start injection earlier. If you want less beam you must start injection later.
  - (beam & RF gates grow “backwards” in time)

Timing System Components



Timing System Components

- Real-Time Data Link (RTDL)
  - Transmits machine parameters and data prior to every new cycle.
  - Each frame contains an 8-bit frame number, 24-bits of data, and an 8-bit CRC.
  - Clock is 10 MHz.
- Event Link
  - Transmits the timing events that define a machine cycle.
  - Each event is 8 bits plus parity (256 events maximum).
  - Clock is variable and derived from the ring revolution frequency ($32 * F_{rev}$).
  - Events 0 – 63 are generated by the timing system hardware.
  - Events 64 – 255 are generated by software (no fixed times).

Hardware Event Assignments

1. Cycle Start
2. Alternate Cycle Start (negative zero crossing)
3. MPS Auto-Reset Fault
4. MPS Latched Fault
27. Source RF
28. Warm Linac High-Power RF
29. Warm Linac Low-Level RF
30. Cold Linac High-Power RF
31. Cold Linac Low-Level RF
32. HEBT High-Power RF
33. HEBT Low-Level RF
36. Beam On
37. Beam Inject
38. End Injection
39. Extract
40. Kicker Charge
43. RTDL Transmit
44. RTDL Valid
45. Data Acquisition “Snapshot” Event
46. Data Acquisition Slow Event (1 Hz)
47. Data Acquisition Fast Event (6 Hz)
48. Save Data
50. RF Sample Trigger

51-59. Reserved (other system triggers)

Software Event Assignments

254. Utility Module Error Counter Reset
253. MPS Error Counter Reset
252. New Event Rep-Rates Set
251. Begin Setting New Event Rep-Rates

Sample RTDL Data Frames (24 bits + 8 bit CRC per frame)

Frame Number	Data
1 – 3	Time of day
4	Event link period
5	MPS mode
6	60 Hz phase error
15	IOC Reset Address
17	Pulse Flavor
24	Previous Pulse Status
25	Cycle
255	24-bit CRC (calculated)

Pulse Flavors

- Eight definable beam profile “Flavors”
- Used by the LEBT chopper to determine beam parameters (index into a set of waveform records).
  - Macropulse width
  - Minipulse width, phase delay, blanking, ramp rates, etc.
- Used by the LLRF to do adaptive tuning.
- Utility Module software uses this parameter to selectively trigger “flavored” read records
- Flavor of each cycle is transmitted on the RTDL (frame 17)

Pulse Flavor Assignments

0 = Beam Off

1 = Target 1 Normal Beam

2 = Target 2 Normal Beam

3 = 10 μSecond Diagnostic Pulse

4 = 50 μSecond Diagnostic Pulse

5 = 100 μSecond Diagnostic Pulse

6 = Physics Pulse

7 = Arbitrary

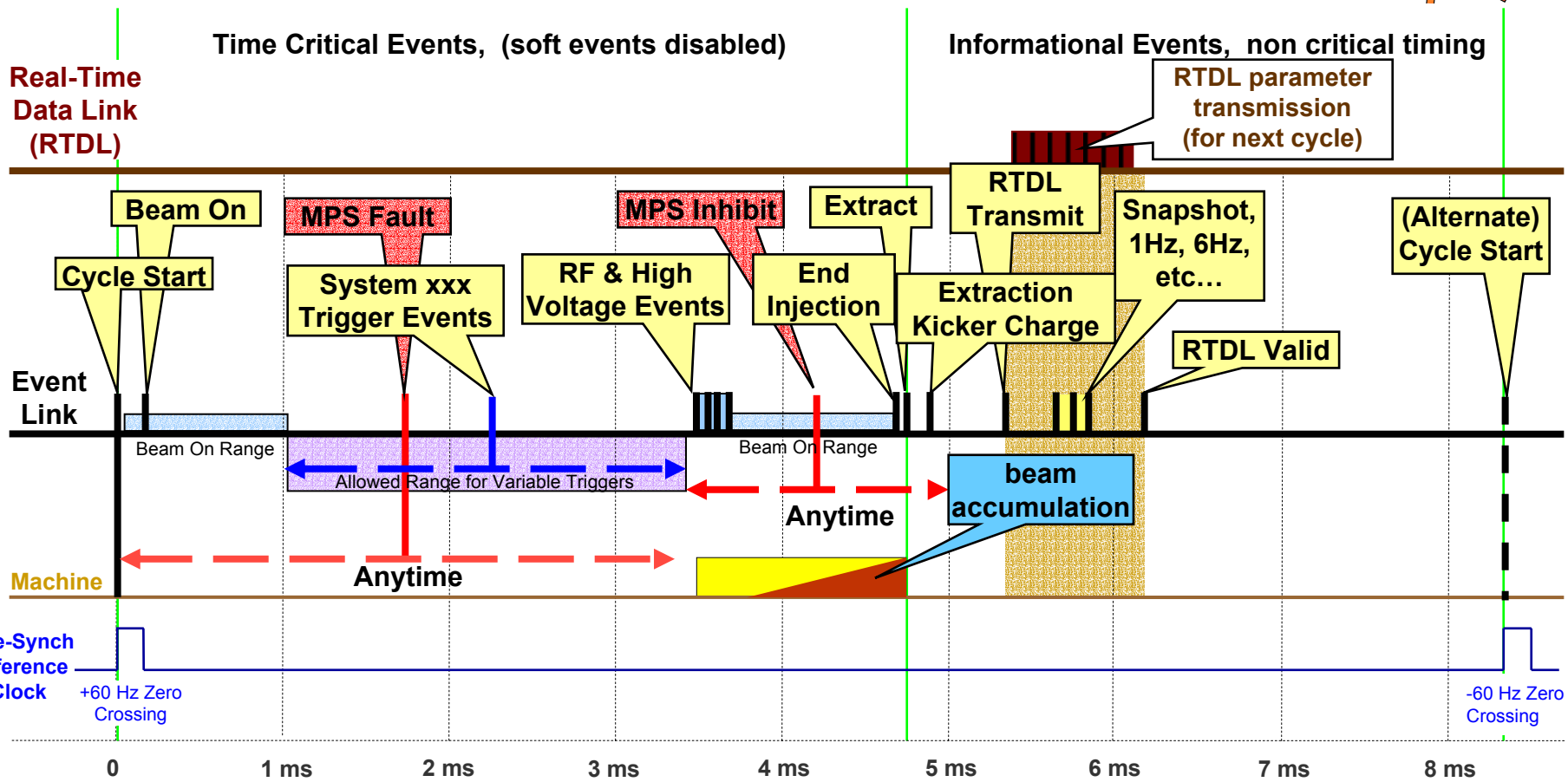
Pulse Flavors

- Four “Normal” Flavors
  1 = Target 1 Normal Beam
  3 = 10 μSecond Diagnostic Pulse
  4 = 50 μSecond Diagnostic Pulse
  5 = 100 μSecond Diagnostic Pulse
- These flavors represent the “normal” beam currently being generated and delivered. They are mutually exclusive and are not “scheduled” on a pulse-to-pulse basis by the timing sequencer.

Pulse Flavors

- Two “Cycle Stealing” Flavors
  6 = Physics Pulse
  7 = Arbitrary
- These flavors are scheduled by the timing scheduler. They typically run in “single-shot” mode or at very low rep-rates. When scheduled, they “steal” machine cycles from the normal beam flavor.

Timeline (from the timing system point of view)



Timing System Components — RTDL

- RTDL Master Module (V105S)
  - VME Module
  - Generates the 10 MHz RTDL Carrier Signal and the RTDL frames.
- RTDL Input Module (V106S / V206S)
  - VME Module
  - Stores the data frames to be sent each cycle on the RTDL.
  - Communicates with the RTDL master module over the VME P2 backplane.
  - V106S contains two frames per module. V206S contains eight frames per module.

Timing System Components — Event Link

- Event Link Master Module (V123S)
  - VME Module.
  - Generates event link carrier (~17 Mhz).
  - Accepts, prioritizes, and transmits “hardware” and “software” events.
- Event Link Input Module (V101S / V201S)
  - VME Module for generating “hardware” events.
  - Communicates with the event link master module over the VME P2 backplane.
  - Hardware events generated from TTL inputs to the V101S / V201S
  - 16 events per module.
  - V201S is a faster version of the V101S.

Timing System Components — Client

- Timing Gate Generator (V124S)
  - Generates TTL timing gates at the local hardware.
  - Responds to triggers from:
    - Event-Link Events
    - External Signals
    - “Manual” Triggers (from programmed VME commands)
  - Independently programmable width, delay, and trigger counts.
- Utility Module
  - Listens to the RTDL and the Event Link.
  - Can generate receipt-of-event interrupts.
  - Handles data timestamping and triggering of “flavored” data.
  - Monitors the health of the VME crate.

Timing System Components — Client

- V294 TTL Fanout Module
  - Single width VME card. No VME interface.
  - V124S card outputs can only drive a single 50 Ω load.
  - Can be re-programmed for functions other than fanout.
- V128 “Smart” Fanout Module
  - Like V294, but can be programmed from the VME bus.

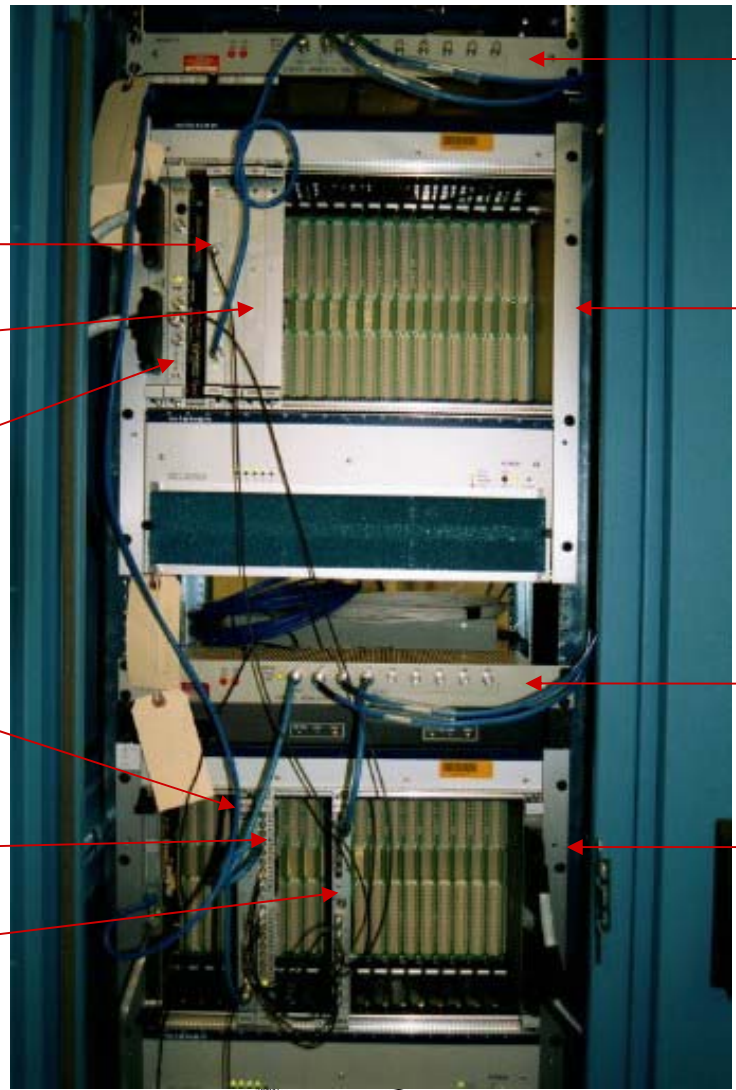
Timing System Components — Other

- Timing Reference Generator
  - Double-Wide VME module.
  - Provides the 60 Hz “Cycle-Start” signal to the event link master module (V123S).
  - Uses a PLL to track the AC line zero-crossing and “smooth out” power grid frequency fluctuations.
  - Resolves the “conflict of interest” between power supplies that need to be “line locked” and the neutron choppers’ need for stable timing.
- Frequency Counter
  - VME Module in the Timing Master crate.
  - Used to monitor the frequency of the event link clock.
  - Frequency is broadcast on the RTDL and sent to the timing reference generator to compensate for changes in the ring revolution frequency.

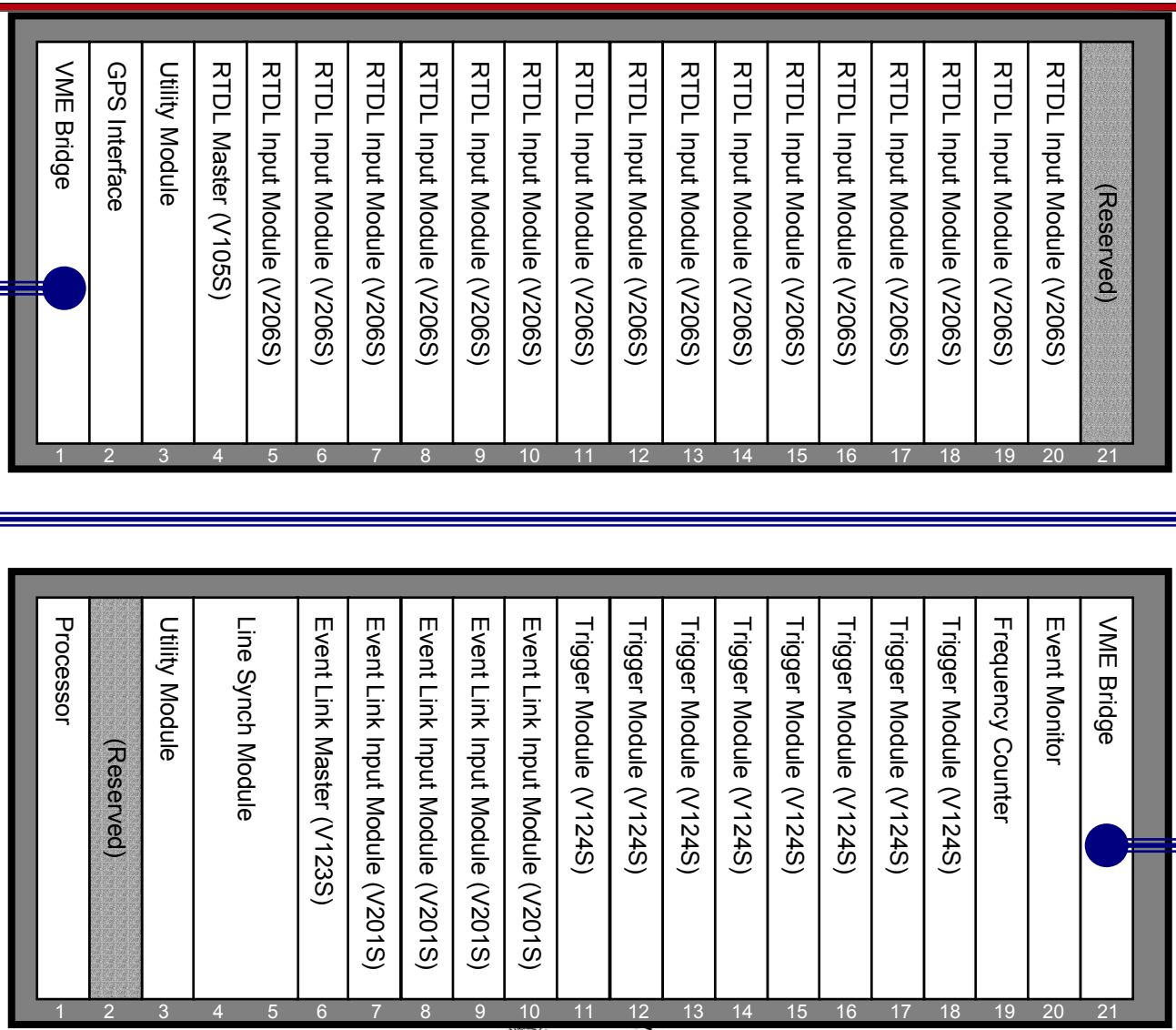
Timing System Components — Other

- GPS and GPS Interface Module
  - GPS provides time source and NTP time service to the site computers.
  - VME interface card captures the GPS time at each “Cycle Start” time.
  - Captured time is sent out on the RTDL.
- Time Line Monitor
  - Monitors the event link and records which events occurred and when.
  - Buffers one full “Super-Cycle” (10 seconds).
  - Used by timing master to make sure the event link is correct.

Timing Master Crate Layout (current)



Timing Master Crate Layout (future)



Operator Interface

Gate/Event Parameters That An Operator Might Typically Control

- Delay
  - Coarse (Turns)
  - Medium ($^1/_{32}$ Turn)
  - Fine (0.5 nanoseconds)
- Width
  - $^1/_{32}$ Turn Resolution
- Rep-Rate
  - 0 – 60 Hz.
  - 0.1 Hz Resolution
  - There are gate/event dependencies
  - Beam gates may only fire at rep-rates less than or equal to the RF rep-rates
  - To keep all gates synchronized, operator must first set desired rep-rates, then press the “Set New Rep-Rates” button.

Gate/Event Parameters That An Operator Typically Does Not Control

- Which event triggers the gate.
- Gate polarity.
- How many pulses a gate generates each time it is triggered.

Application: Ion Source Control

Requirements

- Gate should always end at the same time. Increasing the gate width decreases the delay (and vice versa).
- For thermal stability, the ion source RF duty factor should be constant (constant rep-rate and width).
- LEBT chopper is not fail-safe. On cycles when we don't want beam (e.g. Standby Mode, MPS Latched fault, Flavor = 0,) Source RF should run out of phase with the RFQ.

Application: Ion Source Control

Design Strategy

- The phasing of the source and RFQ is an MPS strategy to get around the fact that the LEBT chopper is not fail-safe.
- Special MPS logic box will select either the “Delayed” or the “In Phase” source gate depending on whether beam is scheduled for this pulse, the state of the MPS system, etc.
- Same box also disables the RFQ RF gate on an MPS Latched fault.

Application: Ion Source Control

Events (From Event Link)

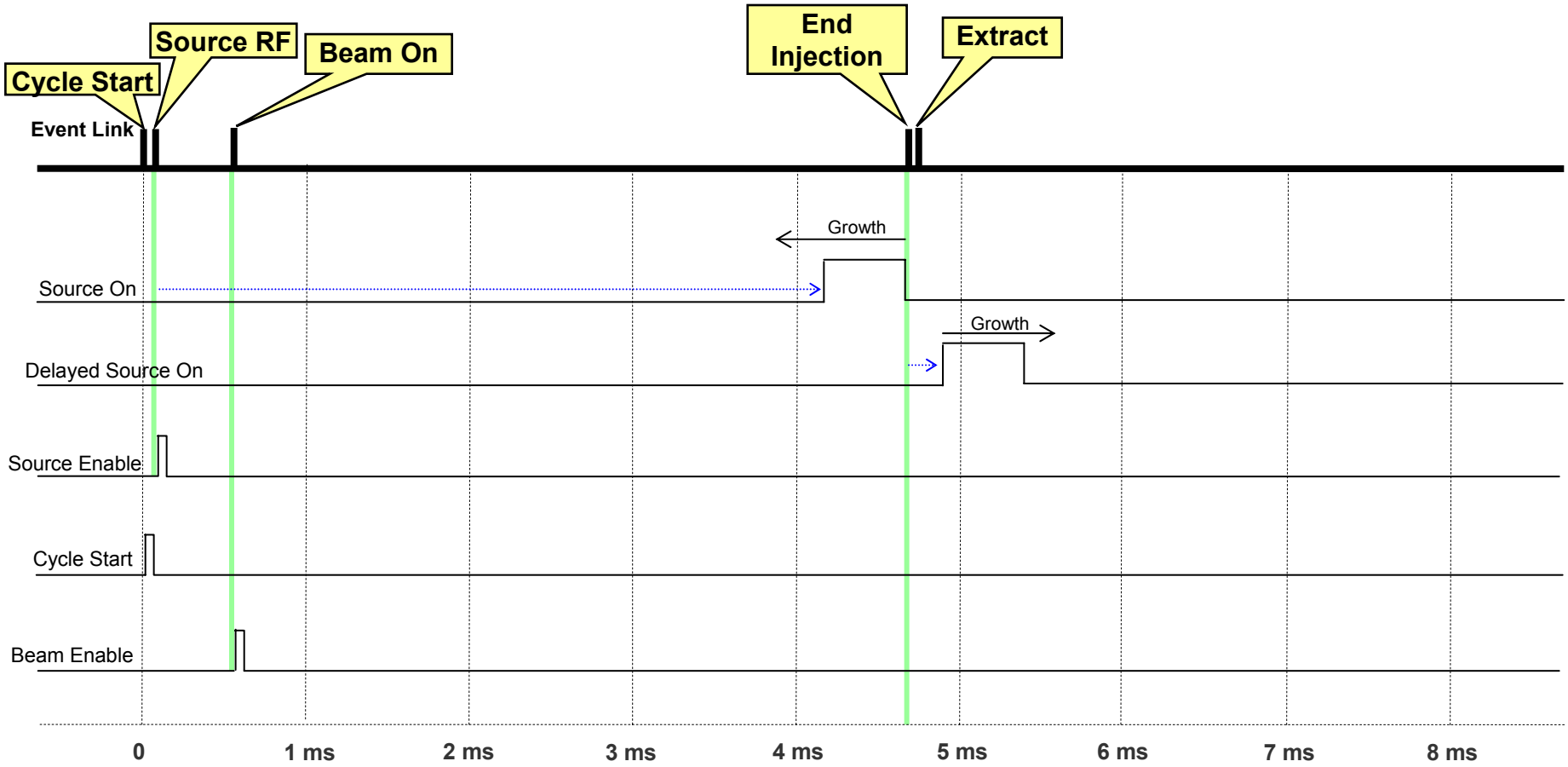
- Source RF Event (27)
  - Variable rep-rate, but usually runs at 60 Hz.
  - Occurs 2 turns after “Cycle Start”
- Beam On Event (36)
  - Variable rep-rate. Synchronous with Source RF cycles (and lots of other events).
  - Occurs 4372 turns (about 4 ms) before beam turns on.
- End Injection Event (38)
  - Fixed Rep-Rate (60 Hz).
  - Occurs ~2 turns before Extract Event.

Application: Ion Source Control

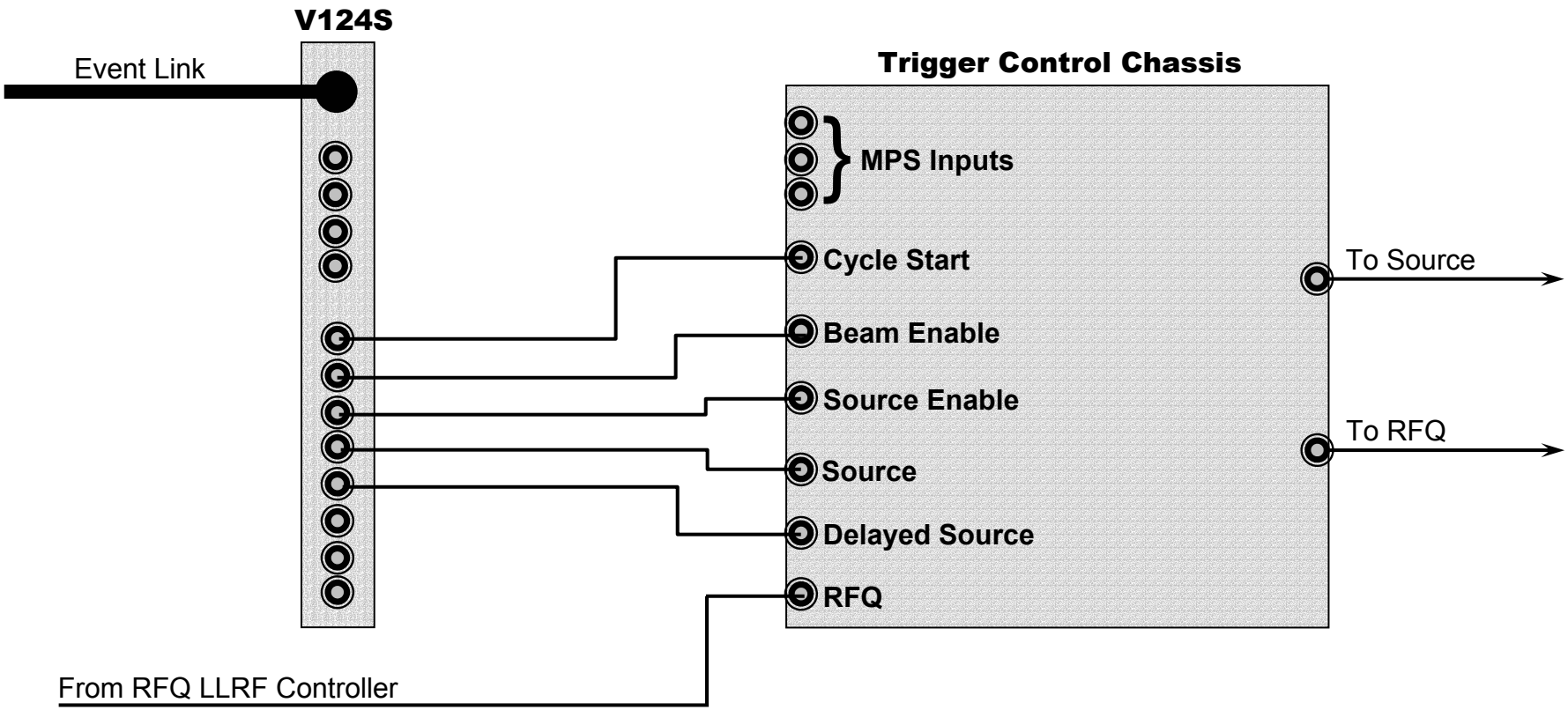
Gates (Generated Locally)

- Source
  - Triggered by “Source RF” Event (variable rep-rate)
  - Delay & width adjusted to end at the “End Injection” event
- Delayed Source
  - Triggered by “End Injection” event (60 Hz)
  - Same width as “Source” Gate
  - Constant delay (long enough to occur after the RFQ turn-off transient)
- Source Enable
  - Triggered by “Source RF” Event
  - No delay, short width. Enables Source output from Trigger Control Chassis.
- Beam Enable
  - Triggered by “Beam On” event (variable rep-rate)
  - No delay, short width (only used to flag “beam on” cycles)
- Cycle Start
  - Triggered by “Cycle Start” event (60 Hz)
  - No delay, short width (used to reset the “trigger control” logic)

Application: Ion Source Control

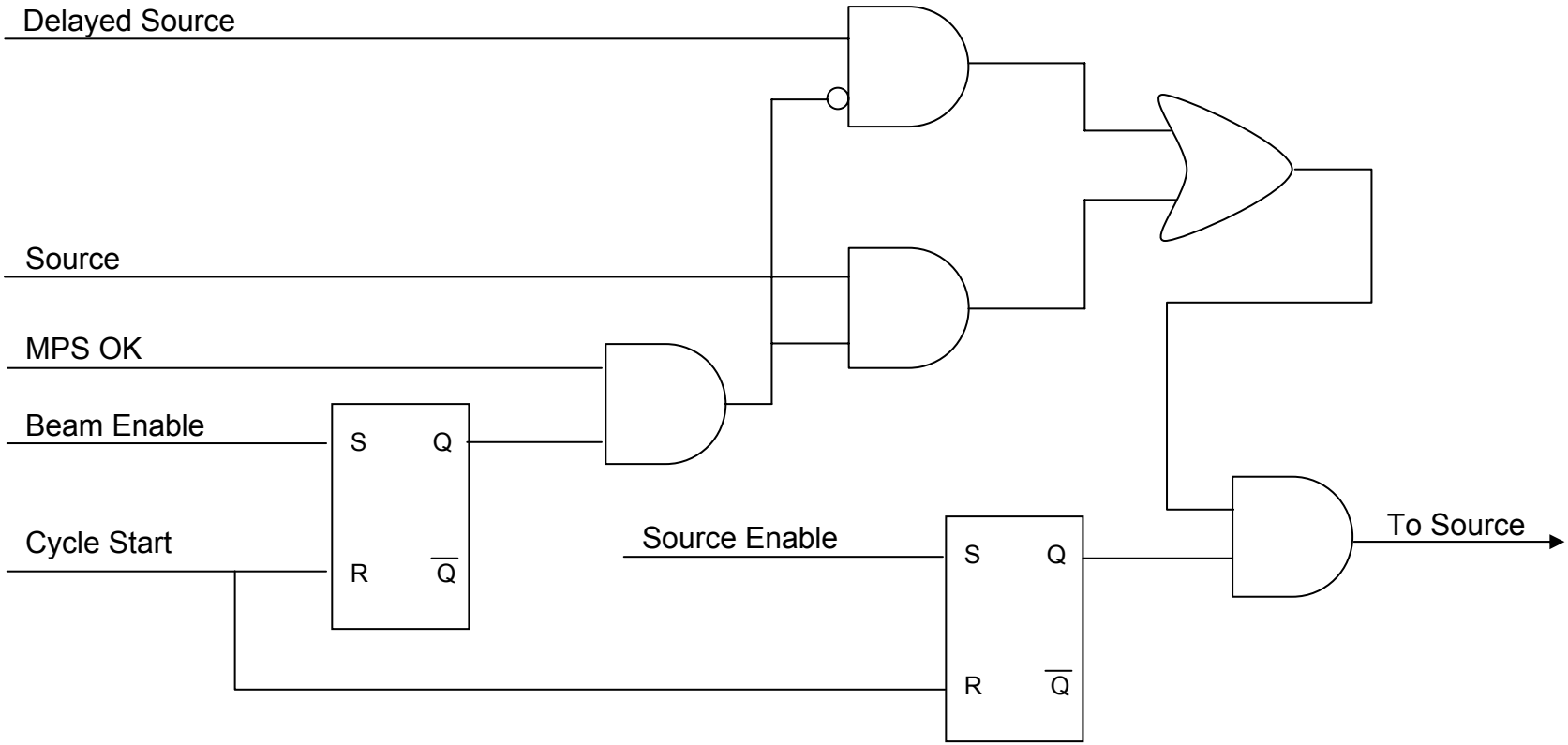


Application: Ion Source Control



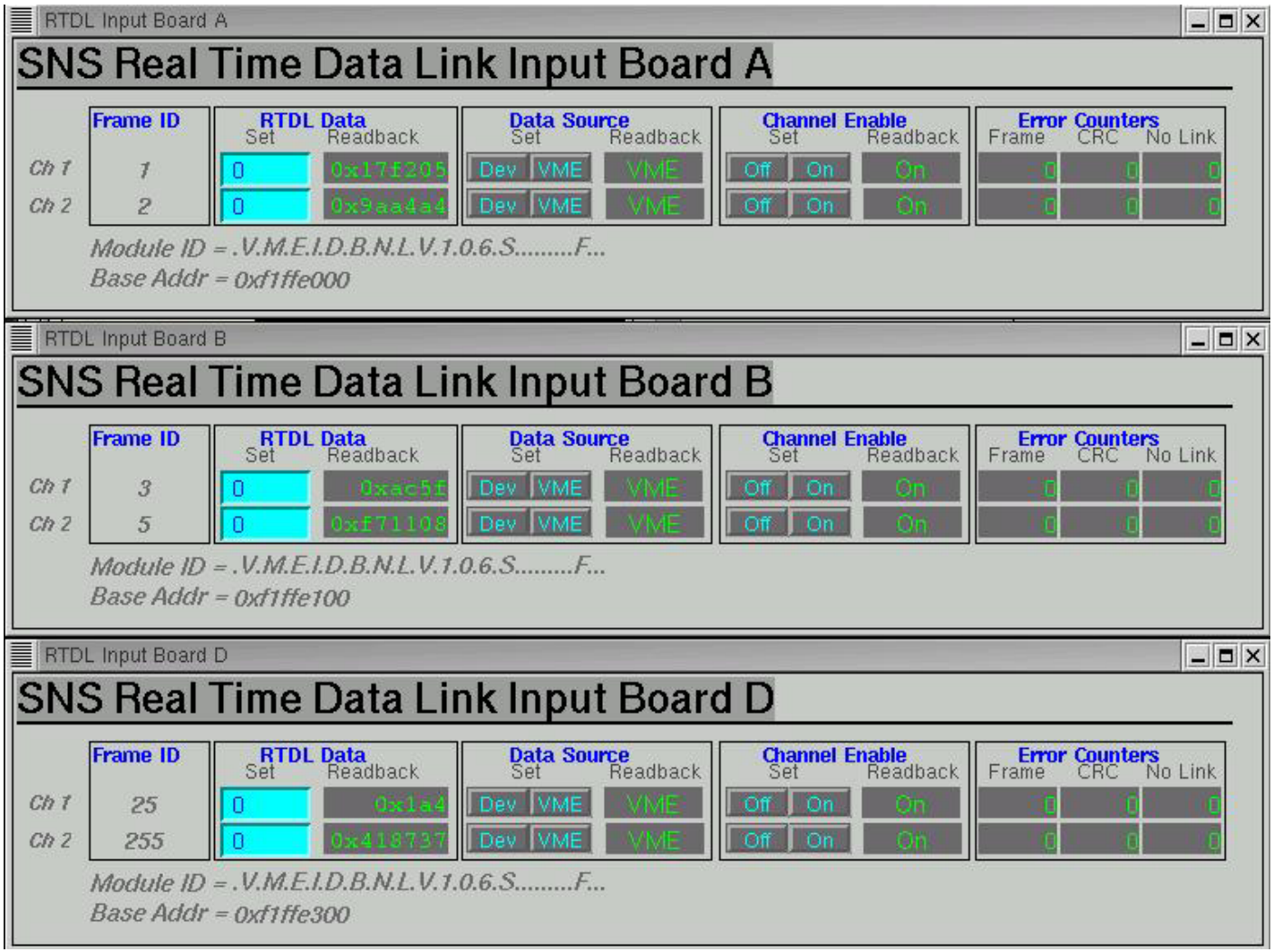
Application: Ion Source Control

Trigger Control Chassis Logic (simplified)

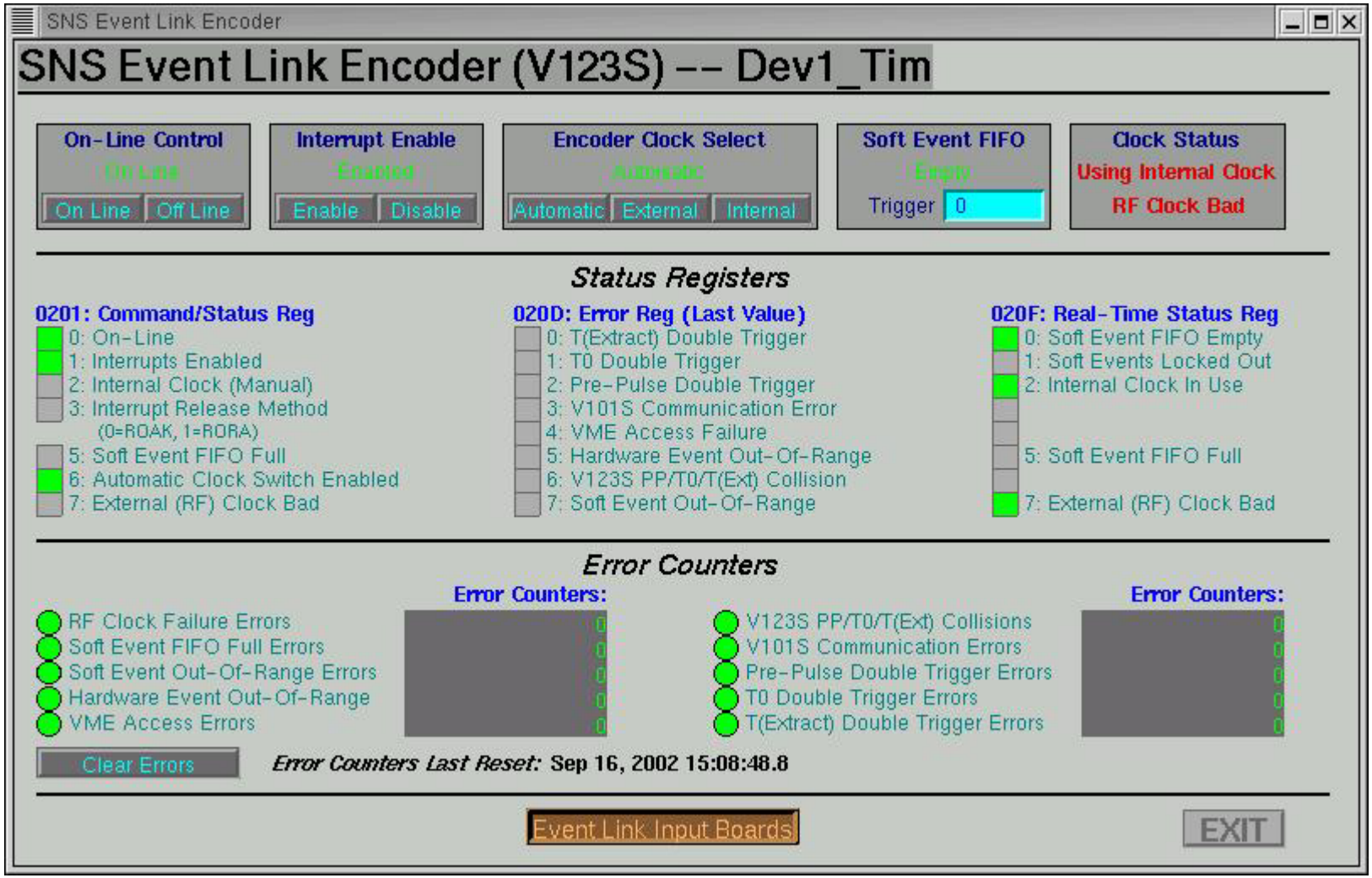


Application: Ion Source Control

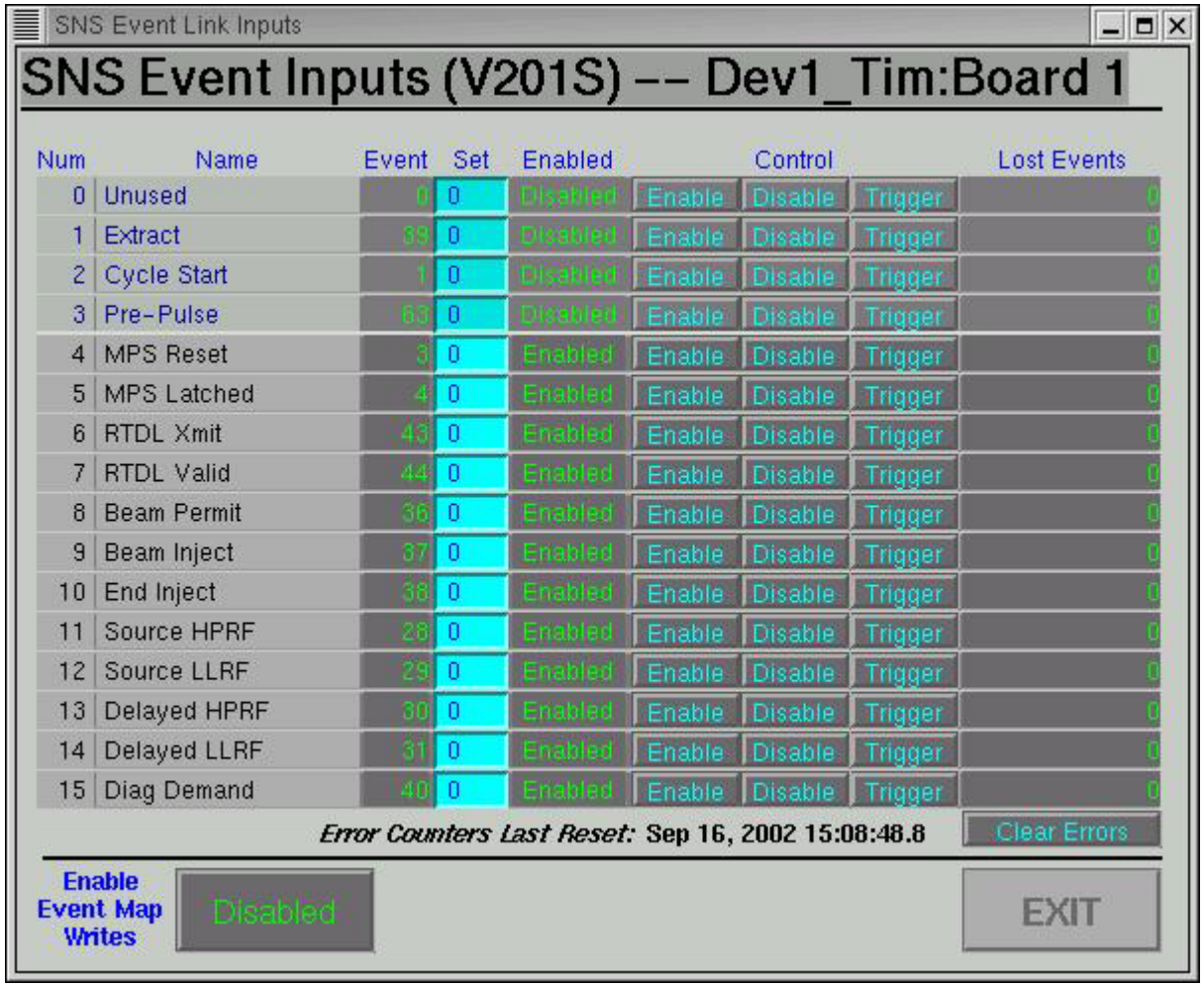
Timing System Debug Screens: RTDL



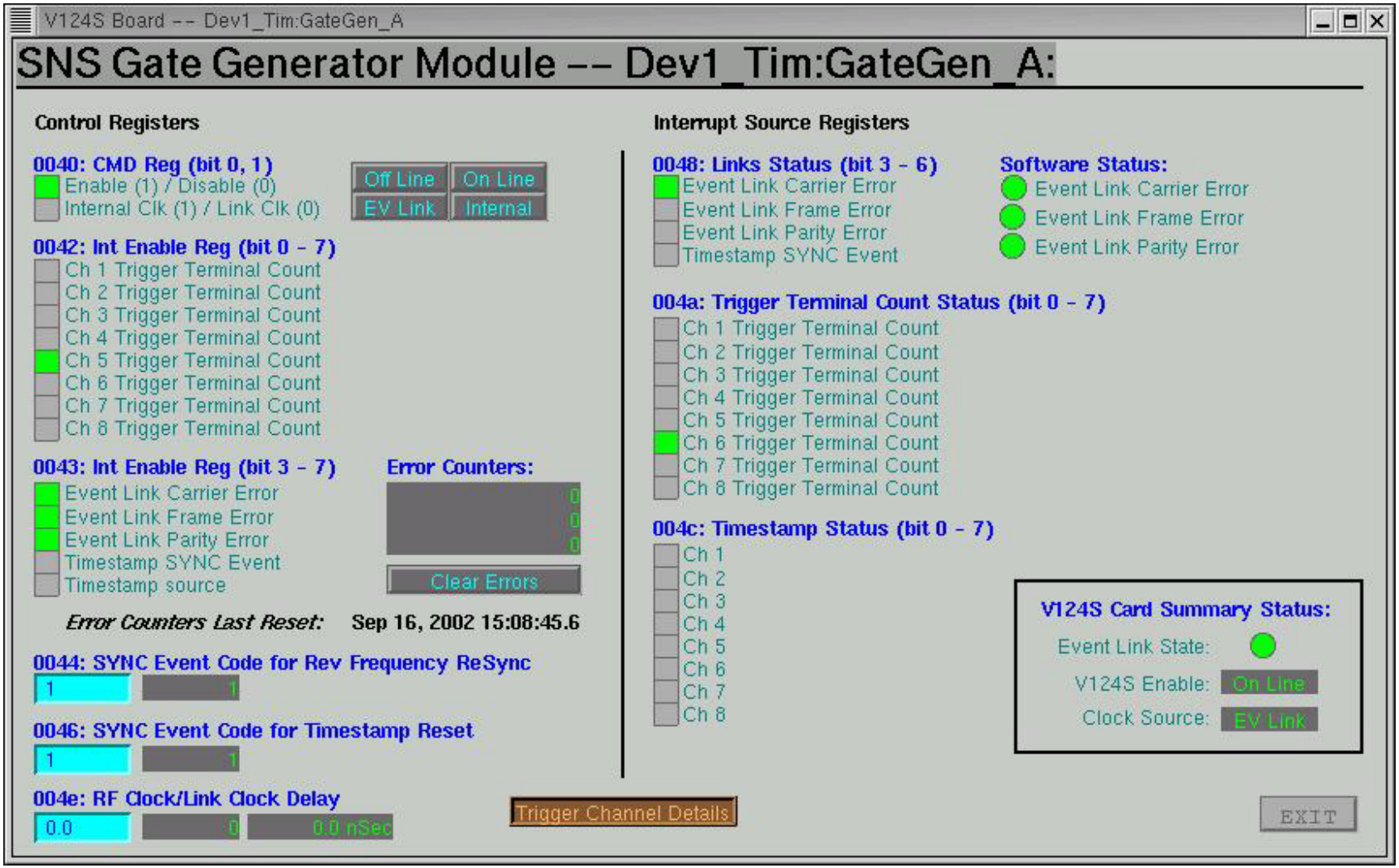
Timing System Debug Screens: Event Master (V123S)



Timing System Debug Screens: Event Input (V201S)



Timing System Debug Screens: Trigger Generator (V124S)



Timing System Debug Screens: Timing Channel (V124S)